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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Patent Application Serial No. .... 10/749,659  
Filing Date ..... December 30, 2003  
Inventor ..... Zhongze Wang  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2812  
Examiner ..... Jennifer M. Kennedy  
Attorney Docket No. .... MI22-2477  
Customer No. .... 021587  
Title ..... Silicon-on-Insulator Comprising Integrated Circuitry

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

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2. Transmittal Form
3. Statement of the Substance of the Interview

Dated: 10/21/04

By:



Pat Palmer  
Telephone No. (509) 624-4276  
Facsimile No. (509) 838-3424

**NUMBER OF PAGES IN FACSIMILE: 5**

PTO/SB/21 (09-04)

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## TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages In This Submission

Application Number	10/749,659
Filing Date	December 30, 2003
First Named Inventor	Zhengze Wang
Art Unit	2812
Examiner Name	Jennifer M. Kennedy
Total Number of Pages In This Submission	MI22-2477

### ENCLOSURES (Check all that apply)

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<input type="checkbox"/> After Final	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Proprietary Information
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### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Wells St. John P.S.		
Signature			
Printed name	Mark S. Malkin		
Date	10/21/04	Reg. No.	32,268

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .... 10/749,659  
Filing Date ..... December 30, 2003  
Inventor ..... Zhongze Wang  
Assignee..... Micron Technology, Inc.  
Group Art Unit..... 2812  
Examiner ..... Jennifer M. Kennedy  
Attorney's Docket No. .... MI22-2477  
Customer No. .... 021567  
Title ..... Silicon-on-Insulator Comprising Integrated Circuitry

**STATEMENT OF THE SUBSTANCE OF THE INTERVIEW**

To: Commissioner for Patents  
**ATTENTION:** Examiner Jennifer M. Kennedy  
Group Art Unit 2812  
P. O. Box 1450  
Alexandria, VA 22313-1450 **VIA FACSIMILE**

From: Mark Matkin (Tel. 509-624-4276; Fax 509-838-3424)  
Wells St. John P.S.  
601 West First Avenue, Suite 1300  
Spokane, WA 99201-3828

An interview was conducted between the undersigned and Examiner Kennedy on October 18, 2004.

It was agreed during the interview that claims 11 and 62 as presented below would be allowable (subject to further searching), and that such amendments would be made/entered by the Examiner by an "Examiner's Amendment".

11. Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along ~~only a portion at least a portion~~ of the channel region between the source/drain regions, a silicon nitride comprising region in contact with the first silicon dioxide comprising region and running along ~~at least a portion~~ only a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

62. Silicon-on-insulator comprising integrated circuitry,  
comprising:

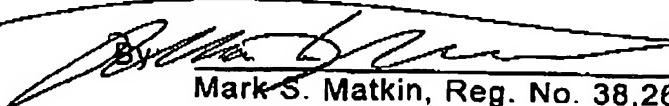
a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along ~~only~~ a portion at least a portion of the channel region between the source/drain regions, a silicon oxynitride comprising region in contact with the first silicon dioxide comprising region and running along ~~at least a portion~~ only a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon oxynitride comprising region, the silicon oxynitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

Respectfully submitted,

Dated: 10-21-04

  
Mark S. Matkin, Reg. No. 38,268